ABSTRACT

The present invention relates to a decoding method and a decoding apparatus in which, while the circuit scale is suppressed, the operating frequency can be suppressed within

5   a sufficiently feasible range, and control of memory access can be performed easily, and to a program therefor. By using a transformation check matrix obtained by performing one of or both a row permutation and a column permutation on an original check matrix of LDPC (Low Density Parity Check)

10   codes, the LDPC codes are decoded. In this case, by using, as a formation matrix, a P × P unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which the unit matrix or the quasi-unit matrix is cyclically

15   shifted, a sum matrix, which is the sum of two or more of the unit matrix, the quasi-unit matrix, and the shift matrix, and a P × P 0-matrix, the transformation check matrix is represented by a combination of a plurality of the formation matrices. A check node calculator 302 simultaneously

20   performs p check node calculations. A variable node calculator 304 simultaneously performs p variable node calculations.